LISTING OF CLAIMS

1. (Original) A semiconductor device comprising:

a first well connected to a pad to which an external pin is connected, the first well including a first-type diffusion region that receives a well bias voltage;

a second well adjacent to the first well, the second well including an insulating region and at least one second-type diffusion region outside the insulating region; and

a third well adjacent to the second well and including a first-type diffusion region that receives a first voltage,

wherein the insulating region inside the second well along with the first-type diffusion region of the first well constitute a bipolar junction transistor which cuts off current from flowing from the first well to the third well.

2. (original) The semiconductor device of claim 1, wherein the at least one second-type diffusion region outside the insulating region comprises a first second-type diffusion region and a second second-type diffusion region, and the second well comprises:

a first sub-well arranged between the insulating region and the first well and including the first second-type diffusion region; and

a second sub-well arranged between the insulating region and the third well and including the second second-type diffusion region,

wherein the insulating region is a third sub-well having a first-type diffusion region.

3. (original) The semiconductor device of claim 2, wherein the first and second sub-wells of the second well are P-wells, and the first voltage is applied to the second-type diffusion regions of the first and second sub-wells of the second well.

4. (Original) The semiconductor device of claim 2, wherein the third sub-well is an N-well, and a second voltage is applied to the first-type diffusion region of the third sub-well.

5. (original) The semiconductor device of claim 4, wherein the first voltage is a ground voltage, and the second voltage generates a backward voltage between a base and an emitter of a bipolar junction transistor, the bipolar junction transistor comprising the first-type diffusion region of the first well, the second-type diffusion region of the first sub-well, and the first-type diffusion region of the third sub-well.

6. (original) The semiconductor device of claim 1, wherein the first and third wells are N-wells.

7. (original) The semiconductor device of claim 1, wherein the well bias voltage applied to the first-type diffusion region of the first well is a power supply voltage.

8. (original) The semiconductor device of claim 1, wherein a region to which the pad is connected is a second-type diffusion region.

9. (original) The semiconductor device of claim 1, wherein the first-type diffusion regions are formed of N-type impurities, and the at least one second-type diffusion region is formed of P-type impurities.

10. (original) The semiconductor device of claim 1, wherein the insulating region of the second well has a structure that surrounds the first well.

11. (original) The semiconductor device of claim 1, wherein the third well constitutes a depletion-type MOS transistor.

12. (previously presented) A semiconductor device comprising:

a first N-well connected to a pad to which an external pin is connected, the first N-well including an N-type diffusion region that receives a well bias voltage, and a P-type diffusion region formed in the vicinity of the pad;

a first P-well adjacent to the first N-well, the first P-well including an insulating region and at least one P-type diffusion region that receives a ground voltage outside the insulating region; and

a second N-well adjacent to the first P-well and including an N-type diffusion region that receives the ground voltage,

wherein the insulating region is a sub-N-well embedded within said first P-well and having an N-type diffusion region that receives an off mode control voltage for preventing a latch-up current.

13. (original) The semiconductor device of claim 12, wherein the at least one P-type diffusion region comprises a first P-type diffusion region and a second P-type diffusion region and the first P-well comprises:

a first sub-P-well located between the insulating region and the first N-well and including the first P-type diffusion region; and

a second sub-P-well located between the insulating region and the second N-well and including the second P-type diffusion region.

14. (original) The semiconductor device of claim 13, wherein the N-type diffusion region of the first N-well, the P-type diffusion region of the first sub-P-well, and the N-type diffusion region of the insulating region constitute a bipolar junction transistor which cuts off a current flowing from the first N-well to the second N-well.

15. (original) The semiconductor device of claim 14, wherein the control voltage generates a backward voltage between a base and an emitter of the bipolar junction transistor composed of the N-type diffusion region of the first N-well, the P-type diffusion region of the first sub-P-well, and the N-type diffusion region of the insulating region.

16. (original) The semiconductor device of claim 12, wherein the well bias

voltage applied to the N-type diffusion region of the first N-well is a power supply voltage.

17. (original) The semiconductor device of claim 12, wherein the insulating region of the first P-well has a structure that surrounds the first N-well.

18. (original) The semiconductor device of claim 12, wherein the second N-well constitutes a depletion-type MOS transistor.

19. (Original) A method of forming a semiconductor device comprising:

forming a first well connected to a pad to which an external pin is connected, the first well including a first-type diffusion region that receives a well bias voltage;

forming a second well adjacent to the first well, the second well including an insulating region and at least one second-type diffusion region outside the insulating region; and

forming a third well adjacent to the second well and including a first-type diffusion region that receives a first voltage,

wherein the insulating region inside the second well along with the first-type diffusion region of the first well constitute a bipolar junction transistor which cuts off current flowing from the first well to the third well.

20. (original) The method of claim 19, wherein the at least one second-type diffusion region outside the insulating region comprises a first second-type diffusion region and a second second-type diffusion region, and the step of forming a second well comprises:

forming a first sub-well between the insulating region and the first well, the first sub-well including the first second-type diffusion region; and

forming a second sub-well between the insulating region and the third well, the second sub-well including the second second-type diffusion region,

wherein the insulating region is a third sub-well having a first-type diffusion region.

21. (original) The method of claim 20, wherein the first and second sub-wells of the second well are P-wells, and the first voltage is applied to the second-type diffusion regions of the first and second sub-wells of the second well.

22. (original) The method of claim 20, wherein the third sub-well is an N-well, and a second voltage is applied to the first-type diffusion region of the third sub-well.

23. (original) The method of claim 19, wherein the first and third wells are N-wells.

24. (original) The method of claim 19, wherein the first-type diffusion regions are formed of N-type impurities, and the at least one second-type diffusion region is formed of P-type impurities.